A 256 × 256 Flash-LiDAR SPAD Imager with Distributed Background Suppression and Adaptive Event Detection for Space Applications in 110nm CIS Technology

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***Abstract*—A Flash-LiDAR single-photon avalanche diode (SPAD)-based sensor for space applications is presented. The sensor integrates a matrix of 256 × 256 interconnected pixels implementing a distributed background suppression mechanism, enabling the detection and timestamping of time- and spatial-correlated photons. The in-pixel reconfigurable logic enables short- and long-range dToF operation up to 380 m and 3 km with a timing resolution of 250 ps and 10 ns, respectively. Moreover, a flexible event detection scheme based on either the first or the last detected event allows improvement of the signal-to-noise ratio (SNR) in case of target at different distances with strong background noise, enhancing the noise rejection capability of the sensor. Preliminary experimental results in an indoor test scene demonstrate the 3D imaging capabilities of the proposed sensor with precision below 1.5 cm at 6 m distance for medium albedo target.**

***Index Terms*—Flash LiDAR; CMOS image sensor; SPAD; TDC; DCR; 3D imaging; coincidence detection; background suppression**

I. Introduction

Light Detection and Ranging (LiDAR) sensors are utilized in a wide variety of applications, from advanced driver-assistance systems (ADAS) in the automotive industry to spacecraft navigation systems for planetary exploration and landing operations. Typically, direct time-of-flight (dToF) Flash LiDAR systems combine a laser source with a pixel array sensor, as illustrated in Figure 1. A short pulse of light is emitted by the laser, flooding the scene with photons. The target backscattered photons are collected by the receiving optics along with background-associated photons. Eventually, the sensor extracts the round-trip time associated with each impinging photon, which is later processed to obtain the target distance.

Among the available technologies, pixel arrays incorporating single-photon avalanche diode (SPAD) arrays with time-to-digital converter (TDC) circuitry allow single photon timestamping, effectively enabling 3D imaging over long distances with high accuracy. However, these sensors present several

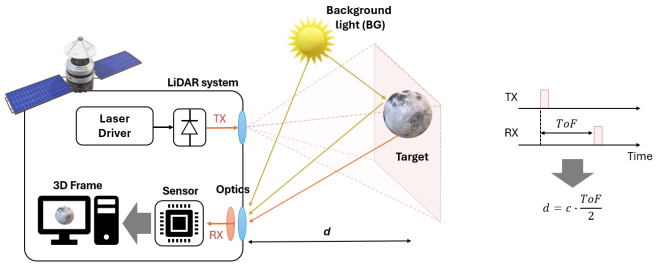

Fig. 1. Flash LiDAR system and operating principle.

trade-offs, including limitations on the maximum achievable distance, tolerance to background light, and frame rate. Moreover, the features packed within a single pixel come at the cost of a larger pixel pitch, which affects the lateral resolution of the final image. Additionally, in space environments, radiation damage can compromise the sensor functionality, making radiation hardness a critical feature for operation under these conditions. Coincidence detection and time gating have been proved effective techniques to mitigate background and dark count rate (DCR) noise.

In [1] a pixel integrating a digital-silicon photomultiplier (d-SiPM) combining the outputs of multiple SPADs, a coincidence detection circuit and a TDC for long-range 3D imaging is proposed achieving limited lateral resolution and fill-factor (FF). Approaches addressing reduced pixel pitch are reported in literature [2], [3] by exploiting a distributed d-SiPM or by sharing the TDC between pixels. Thanks to the advantages brought by 3D-stacking technology, a series of sensor architectures with dedicated sensing and processing tiers have been investigated. These architectures organize SPADs in macro-pixel and shared multi-event TDC, resulting in compact pixel size and high fill-factor [4], [5]. Recently, on-chip and in-pixel histogramming techniques have been adopted to reduce and further compress the amount of data generated by the sensor,

achieving lower power consumption and higher frame rate [6]–[10]. In this work, we present the next development of Flash LiDAR sensor previously presented in [2]. The focal-plane-array is 16 times larger than its predecessor, while most of its features are preserved.

The paper is organized as follows: Section II details the sensor and pixel architecture, along with the peripheral circuitry. Section III presents the results of the electro-optical characterization and preliminary functional characterization. Finally, Section IV summarizes the findings and concludes the work.

II. Sensor Architecture

The sensor architecture is depicted in Figure 2, showing a matrix of 256×256 pixel array, a readout circuitry, a serial-to-parallel interface (SPI) for accessing the configuration registers and PLL-locked TDC.

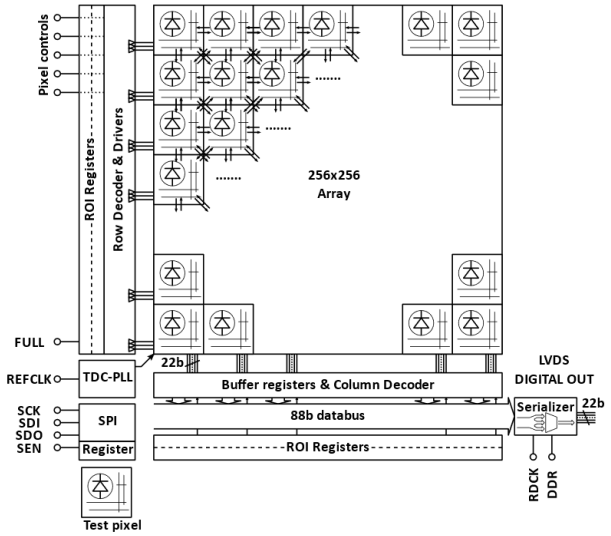

Fig. 2. 256×256 pixel array sensor architecture block diagram.

A. Focal-plane-array (FPA)

The FPA consists of a matrix of 256×256 interconnected pixels implementing the distributed dSiPM concept illustrated in Figure 3 to mitigate background noise. Unlike in [1], each pixel integrates a single SPAD with a dedicated TDC. Given that neighboring pixels typically observe surfaces at comparable distances, coincidence detection is performed simultaneously by all pixels. This is achieved by exploiting the interconnections between neighbors to validate only bursts of time- and spatially-correlated photons. When the primary pixel (P) detects a photon, it looks for validation flags (VALID) generated by neighboring pixels (S) within a short time correlation window (T_{win}). The TDC is triggered only if the number of VALID flags exceeds a user-programmable threshold; otherwise, the event is discarded. This approach allows for higher background noise rejection with a smaller pixel pitch, without compromising lateral resolution.

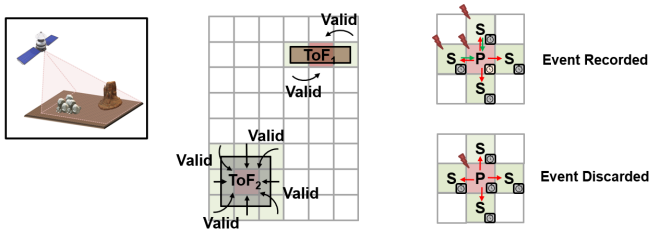

Fig. 3. Distributed digital silicon photomultiplier concept.

B. Pixel

Figure 4 illustrates the pixel block diagram, which integrates an active quenching and recharging front-end (FE) circuit with time-gating, correlation logic, a measurement controller, and a reconfigurable 14-bit current-starved TDC with a memory buffer. The FE output is fed into the correlation logic block and neighboring pixels. The correlation logic generates a trigger (TRIG) for the measurement controller only when an event is validated based on a programmable geometric pattern and threshold (THR).

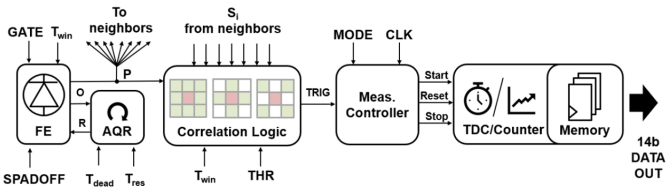

Fig. 4. Pixel architecture block diagram.

The measurement controller manages the start, stop and reset signals for the TDC. Two different ranging modes, named altimeter and imager, allow short- and long- range dToF operation up to 380 m and 3 km respectively, with a timing resolution of 250 ps and 10 ns. Additionally, the sensor can perform single photon counting operation up to 2047 photons within a given time gating window. As illustrated in Figure 5 and demonstrated in [2], [11], a flexible detection strategy based on first and last-hit detection schemes allows improvement of the signal-to-noise ratio (SNR) in case of targets at varying distances and under strong background noise, enhancing the noise rejection capability of the sensor. To further reduce the pixel pitch, the automatic-sensitivity feature was removed from the current implementation, due to the limited improvement in SNR.

C. Periphery

The pixel array is surrounded by readout and driving circuitry. Decoders select rows and columns for readout based on the region of interest (ROI) registers, while a fast-serializer outputs data via a 22-lane LVDS in single- or double- data rate mode. A fast-readout mode enables the simultaneous readout of two consecutive rows, accommodating 11-b of the pixel timestamp in the output data bus. When enabled, this feature reduces the short- and long- maximum distance

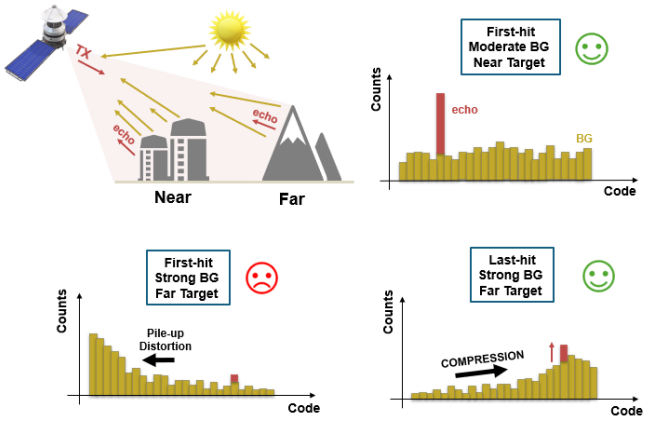

Fig. 5. Pixel event detection strategies based on first and last hit.

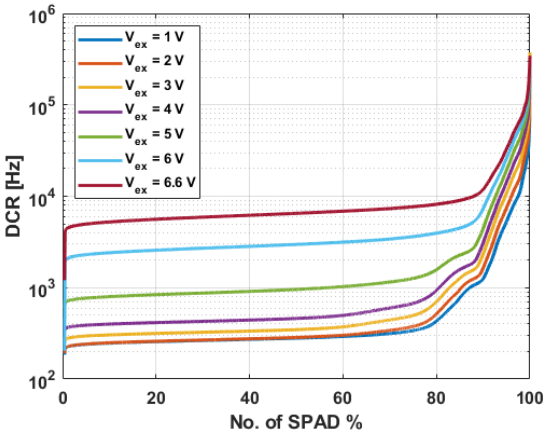

Fig. 7. Sorted cumulative distribution of the SPAD DCR.

range to 48 m and 384 m, respectively, but halves the readout time when higher precision or fast acquisition is required. The chip includes an SPI for sensor configuration and ROI programming. Peripheral circuits are implemented with rad-hard techniques to reduce radiation damage. A PLL-locked TDC replica at the chip edge ensures timing stability against PVT variations.

III. Preliminary Experimental Results

Figure 6 shows the 1.2×1.2 cm pixel array fabricated in 110 nm CMOS image sensor (CIS) technology, featuring a $44\,\mu$m pixel pitch with a $17.5\,\%$ fill-factor, including the SPAD, the pixel logic, the 14-b TDC, and the memory buffer.

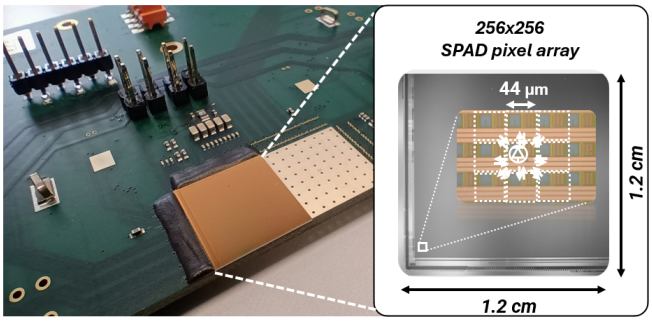

Fig. 6. Fabricated SPAD-based flash LiDAR sensor with the chip micrograph.

A. SPAD DCR Characterization

Figure 7 shows the sorted cumulative distribution of the SPAD DCR for different excess voltages at room temperature. The median and mean DCR values are equal to 6.5 kHz and 10.7 kHz at 6.6 V excess bias voltage V_{ex}, applied over a the breakdown voltage of 20.5 V. The resulting DCR is higher than similar SPADs realized in the same technology [2] which can be attribuited to a non-uniform distribution of the SPAD cathode voltage, with some pixels experiencing higher V_{ex}.

B. TDC Characterization and Timing Performance

The TDC linearity and full-scale value (LSB) are characterized by means of a code density test. The differential and integral non-linearity (DNL, INL) metrics are extracted, setting the reference LSB to 250 ps by means of the external PLL-locked TDC. Figure 8 shows a measurement of DNL and INL for a typical pixel, removing the bins at the edges which are affected by poor statistics. The high non-linearity (> 0.5 LSB) can be attributed to the supply fluctuations due to the power consumption and distribution of the coarse high-frequency clock.

The single-photon timing resolution (SPTR) is extracted by illuminating the sensor with a 470 nm, 70 ps FWHM laser source, resulting in an average of about 315 ps FWHM, including SPAD, in-pixel electronics, and TDC jitters.

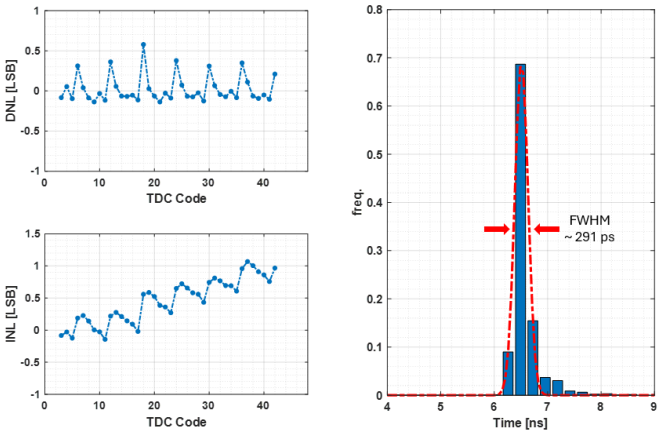

Fig. 8. Typical pixel timing performance, including differential and integral non-linearity (DNL, INL) and single photon timing resolution (SPTR).

C. Functional Characterization

A preliminary depth map of an indoor test scene is shown in Figure 9 acquired using 532 nm, 1 ns FWHM and diffused laser source. Off-the-shelf optics are used setting a FOV equal

to 20 × 20°. The sensor is configured in imager mode, first-hit, with the reference LSB locked at 250 ps. The timestamp histogram is built off-chip for each single pixel with 50 sub-images acquired at 1.4 kfps. After full-scale calibration and DNL compensation, the peak detection algorithm is applied over the calibrated histograms of each pixel to extract the measured distance. The resulting 3D-frame reproduced the reference scene with high detail and fidelity, despite the misalignment between the laser and the sensor, leading to parallax effects. Figure 10 shows another test scene, which

Fig. 9. Reference image and 3D frame.

includes three calibrated targets with albedos of 5%, 50%, and 95%. The standard deviation map was obtained using 100 acquisitions of 100 sub-images each. Precision was calculated by averaging an area of 40×40 pixels, resulting in a precision below 1.4 cm at a 6-meter distance for targets with albedos higher than 50%. For targets with a 5% albedo, the precision exceeded 1 m, primarily due to poor SNR and the failure of the peak detection algorithm.

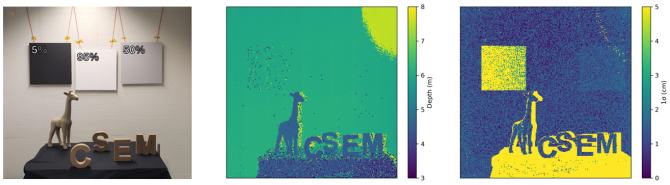

Fig. 10. (a).Reference scene with different target albedos; (b).Depth map; (c).Standard deviation map.

IV. Conclusions

A Flash-LiDAR SPAD-based sensor for space applications, realized in 110 nm CMOS image sensor (CIS) technology, has been presented. The array integrates a matrix of 256 × 256 interconnected pixels, implementing a distributed background suppression mechanism without loss of spatial resolution. This solution enables the detection and timestamping of time- and spatially-correlated photons. Each pixel integrates a single SPAD, a measurement controller, a 14-bit TDC, and a memory buffer within a 44 µm pixel pitch, featuring a 17.5% fill-factor.

The in-pixel reconfigurable logic enables short- and long-range dToF operation up to 380 m and 3 km, respectively, with timing resolutions of 250 ps and 10 ns. Additionally, a flexible event detection scheme based on either the first or last detected event improves the SNR, especially for targets at varying distances with high background noise. Preliminary experimental results in an indoor test scene demonstrate the sensor's 3D imaging capability, achieving a precision below 1.5 cm at a 6 m distance for medium albedo targets.

Acknowledgment

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References

[1] M. Perenzoni, D. Perenzoni, and D. Stoppa, "A 64 × 64-pixels digital silicon photomultiplier direct tof sensor with 100-mphotons/s/pixel background rejection and imaging/altimeter mode with 0.14

[2] E. Manuzzato, A. Tontini, A. Seljak, and M. Perenzoni, "A 64 × 64-pixel flash lidar spad imager with distributed pixel-to-pixel correlation for background rejection, tunable automatic pixel sensitivity and first-last event detection strategies for space applications," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65, pp. 96–98, 2022.

[3] Y. M. Wang, L. Shi, C. Wang, K. O. Kim, I. Ovsiannikov, and S. Hwang, "A direct tof sensor with in-pixel differential time-to-charge converters for automotive flash lidar and other 3d applications," in *Proc. Int. Image Sens. Workshop*, p. R24, 2019.

[4] R. K. Henderson, N. Johnston, S. W. Hutchings, I. Gyongy, T. Al Abbas, N. Dutton, M. Tyler, S. Chan, and J. Leach, "5.7 a 256× 256 40nm/90nm cmos 3d-stacked 120db dynamic-range reconfigurable time-resolved spad imager," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, pp. 106–108, IEEE, 2019.

[5] P. Padmanabhan, C. Zhang, M. Cazzaniga, B. Efe, A. R. Ximenes, M.-J. Lee, and E. Charbon, "7.4 a 256× 128 3d-stacked (45nm) spad flash lidar with 7-level coincidence detection and progressive gating for 100m range and 10klux background light," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, pp. 111–113, IEEE, 2021.

[6] D. Stoppa, S. Abovyan, D. Furrer, R. Gancarz, T. Jessenig, R. Kappel, M. Lueger, C. Mautner, I. Mills, D. Perenzoni, *et al.*, "A reconfigurable qvga/q3vga direct time-of-flight 3d imaging system with on-chip depth-map computation in 45/40 nm 3d-stacked bsi spad cmos," in *Proc. Int. Image Sensor Workshop*, pp. 53–56, 2021.

[7] O. Kumagai, J. Ohmachi, M. Matsumura, S. Yagi, K. Tayu, K. Amagawa, T. Matsukawa, O. Ozawa, D. Hirono, Y. Shinozuka, R. Homma, K. Mahara, T. Ohyama, Y. Morita, S. Shimada, T. Ueno, A. Matsumoto, Y. Otake, T. Wakano, and T. Izawa, "7.3 a 189×600 back-illuminated stacked spad direct time-of-flight depth sensor for automotive lidar systems," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, pp. 110–112, 2021.

[8] S.-H. Han, S. Park, J.-H. Chun, J. Choi, and S.-J. Kim, "6.7 a 160×120 flash lidar sensor with fully analog-assisted in- pixel histogramming tdc based on self-referenced sar adc," in *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 67, pp. 112–114, 2024.

[9] M. Kim, H. Seo, S. Kim, J.-H. Chun, S.-J. Kim, and J. Choi, "6.11 a 320x240 cmos lidar sensor with 6-transistor nmos-only spad analog front-end and area-efficient priority histogram memory," in *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 67, pp. 120–122, 2024.

[10] I. Gyongy, A. T. Erdogan, N. A. Dutton, G. M. Martín, A. Gorman, H. Mai, F. M. D. Rocca, and R. K. Henderson, "A direct time-of-flight image sensor with in-pixel surface detection and dynamic vision," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 30, no. 1: Single-Photon Technologies and Applications, pp. 1–11, 2024.

[11] A. Tontini, L. Gasparini, E. Manuzzato, M. Perenzoni, and R. Passerone, "Comparison of background-rejection techniques for spad-based lidar systems," in *2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, pp. 45–48, 2022.